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Jameco Part Number 1585194

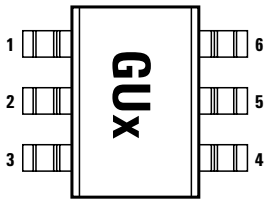
HSMP - 389x & HSMP - 489x Series
Surface Mount RF PIN Switch Diodes

Data Sheet

Description

The HSMP-389x series is optimized for switching applications where low resistance at low current and low capacitance are required. The HSMP-489x series products feature ultra low parasitic inductance. These products are specifically designed for use at frequencies which are much higher than the upper limit for conventional PIN diodes.

Pin Connections and Package Marking



Notes:
1. Package marking provides orientation, identification, and date code.
2. See "Electrical Specifications" for appropriate package marking.

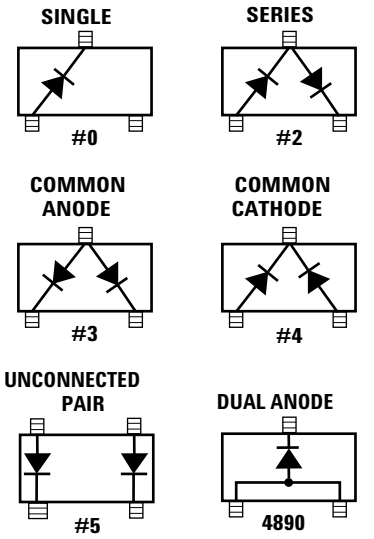
Features

- Unique Configurations in Surface Mount Packages
  - Add Flexibility
  - Save Board Space
  - Reduce Cost
- Switching
  - Low Capacitance
  - Low Resistance at Low Current
- Low Failure in Time (FIT) Rate[1]
- Matched Diodes for Consistent Performance
- Better Thermal Conductivity for Higher Power Dissipation
- Lead-free Option Available

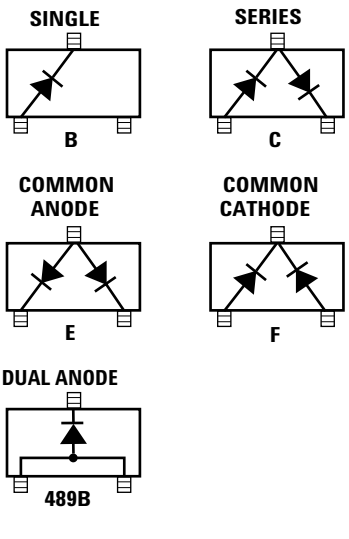
Note:

1. For more information see the Surface Mount PIN Reliability Data Sheet.

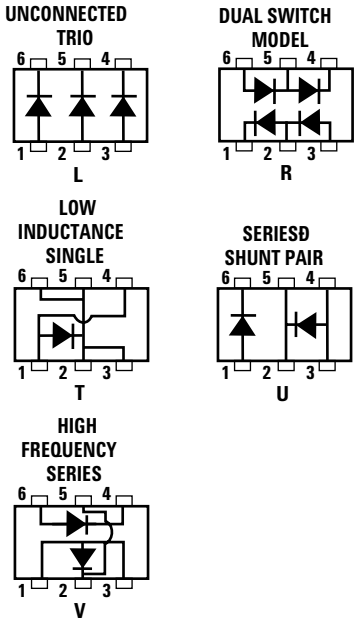
Package Lead Code Identification, SOT-23/143 (Top View)



Package Lead Code Identification, SOT-323 (Top View)



Package Lead Code Identification, SOT-363 (Top View)



ESD WARNING:
Handling Precautions Should Be Taken To Avoid Static Discharge.

Absolute Maximum Ratings[1] $T_C = +25°C$

Symbol	Parameter	Unit	SOT-23/143	SOT-323/363
I_F	Forward Current (1 µs Pulse)	Amp	1	1
P_{IV}	Peak Inverse Voltage	V	100	100
T_j	Junction Temperature	°C	150	150
T_{stg}	Storage Temperature	°C	-65 to 150	-65 to 150
θ_{jc}	Thermal Resistance[2]	°C/W	500	150

Notes:
1. Operation in excess of any one of these conditions may result in permanent damage to the device.
2. $T_C = +25°C$, where T_C is defined to be the temperature at the package pins where contact is made to the circuit board.

Electrical Specifications, T_C = 25°C, each diode

Part Number HSMP-	Package Marking Code	Lead Code	Configuration	Minimum Breakdown Voltage V_{BR} (V)	Maximum Series Resistance R_S (Ω)	Maximum Total Capacitance C_T (pF)
3890 3892 3893 3894 3895 389B 389C 389E 389F 389L 389R 389T 389U 389V	G0 G2 G3 G4 G5 G0 G2 G3 G4 GL S Z GU GV	0 2 3 4 5 B C E F L R T U V	Single Series Common Anode Common Cathode Unconnected Pair Single Series Common Anode Common Cathode Unconnected Trio Dual Switch Mode Low Inductance Single Series-Shunt Pair High Frequency Series Pair	100	2.5	0.30
Test Conditions				$V_R = V_{BR}$ Measure $I_R \leq 10$ µA	I_F = 5 mA f = 100 MHz	V_R = 5 V f = 1 MHz

High Frequency (Low Inductance, 500 MHz–3 GHz) PIN Diodes

Part Number HSMP-	Package Marking Code[1]	Configuration	Minimum Breakdown Voltage V_{BR} (V)	Maximum Series Resistance R_S (Ω)	Typical Total Capacitance C_T (pF)	Maximum Total Capacitance C_T (pF)	Typical Total Inductance L_T (nH)
489x	GA	Dual Anode	100	2.5	0.33	0.375	1.0
Test Conditions			$V_R = V_{BR}$ Measure $I_R \leq 10$ µA	I_F = 5 mA	f = 1 MHz V_R = 5 V	V_R = 5 V f = 1 MHz	f=500 MHz– 3 GHz

Typical Parameters at T_C = 25°C

Part Number HSMP-	Series Resistance R_S (Ω)	Carrier Lifetime τ (ns)	Total Capacitance C_T (pF)
389x	3.8	200	0.20 @ 5V
Test Conditions	I_F = 1 mA f = 100 MHz	I_F = 10 mA I_R = 6 mA	

HSMP-389x Series Typical Performance, T_C = 25°C, each diode

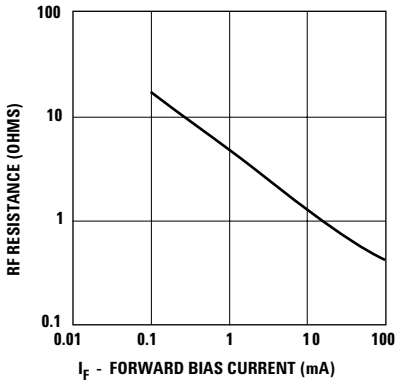


Figure 1. Total RF Resistance at 25 C vs. Forward Bias Current.

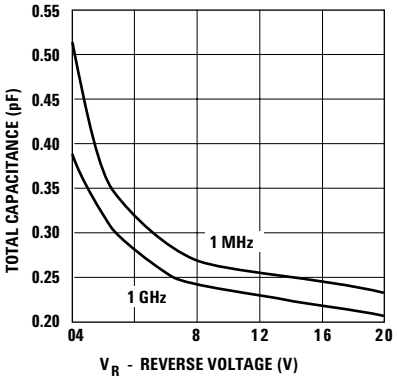


Figure 2. Capacitance vs. Reverse Voltage.

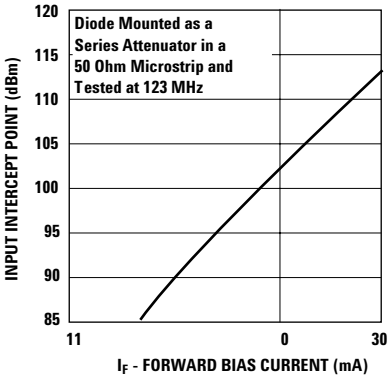


Figure 3. 2nd Harmonic Input Intercept Point vs. Forward Bias Current.

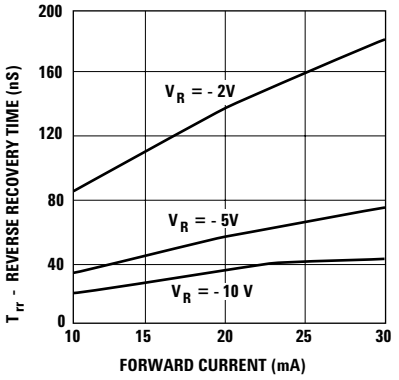


Figure 4. Typical Reverse Recovery Time vs. Reverse Voltage.

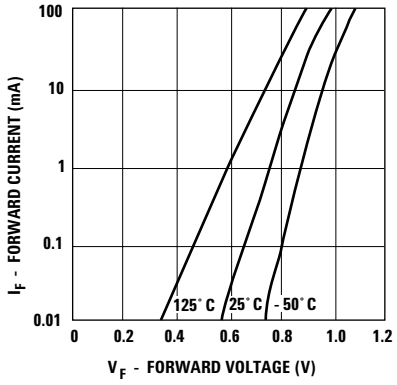


Figure 5. Forward Current vs. Forward Voltage.

Typical Applications for Multiple Diode Products

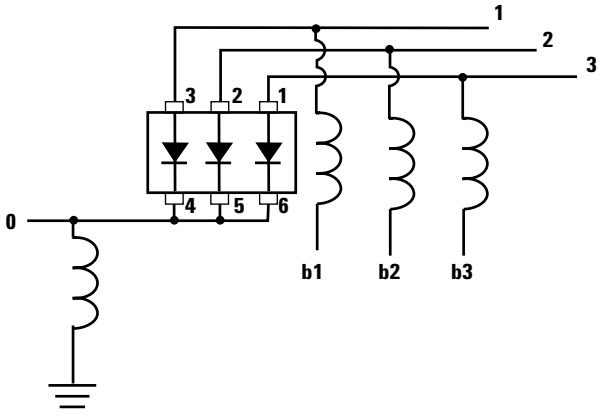
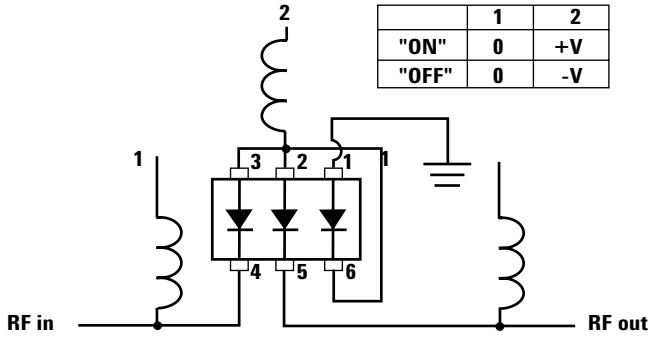


Figure 6. HSMP-389L used in a SP3T Switch.



	1	2
"ON"	0	+V
"OFF"	0	-V

Figure 7. HSMP-389L Unconnected Trio used in a Dual Voltage, High Isolation Switch.

Typical Applications for Multiple Diode Products (continued)

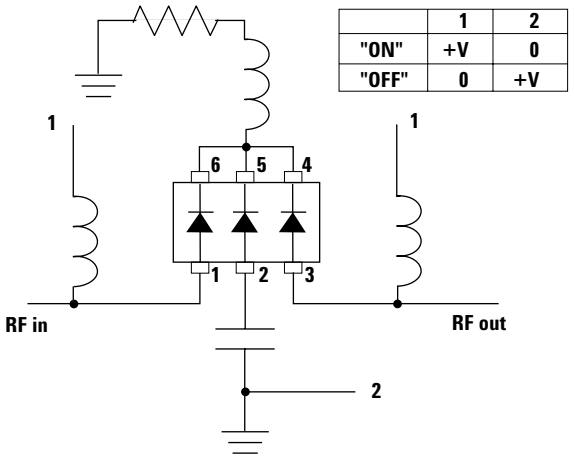


Figure 8. HSMP-389L Unconnected Trio used in a Positive Voltage, High Isolation Switch.

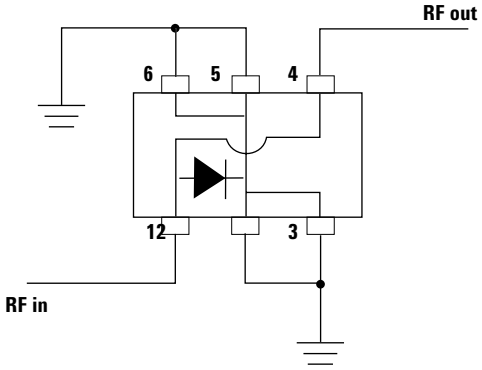


Figure 9. HSMP-389T used in a Low Inductance Shunt Mounted Switch.

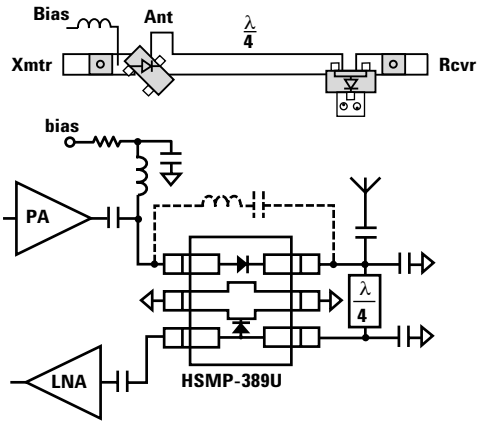


Figure 10. HSMP-389U Series/Shunt Pair used in a 900 MHz Transmit/Receive Switch.

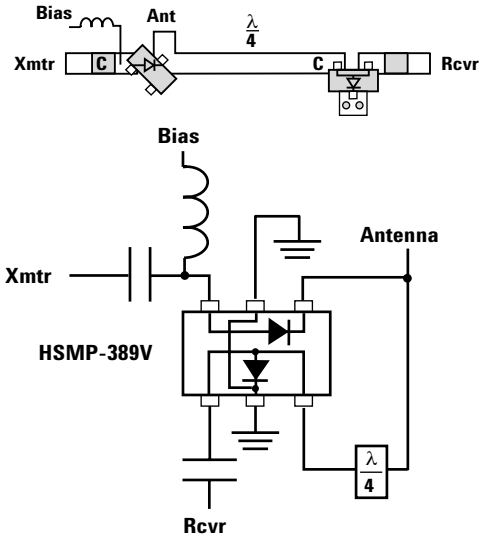


Figure 11. HSMP-389V Series/Shunt Pair used in a 1.8 GHz Transmit/Receive Switch.

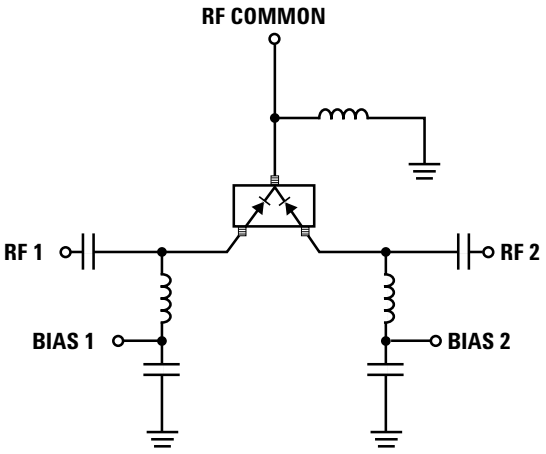


Figure 12. Simple SPDT Switch, Using Only Positive Current.

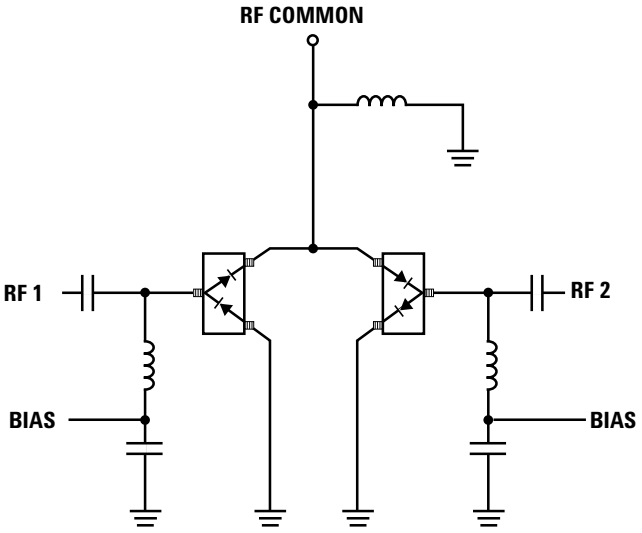


Figure 13. High Isolation SPDT Switch, Dual Bias.

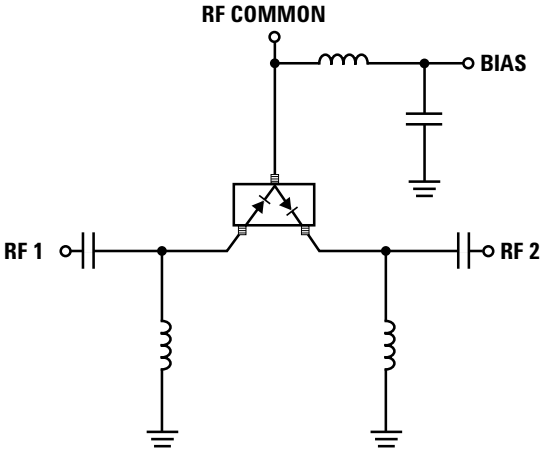


Figure 14. Switch Using Both Positive and Negative Bias Current.

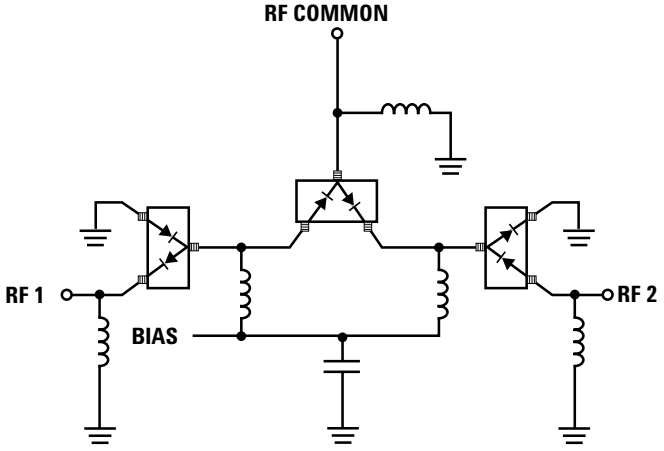


Figure 15. Very High Isolation SPDT Switch, Dual Bias.

Typical Applications for HSMP-489x Low Inductance Series

Microstrip Series Connection for HSMP-489x Series

In order to take full advantage of the low inductance of the HSMP-489x series when using them in series applications, both lead 1 and lead 2 should be connected together, as shown in Figure 17.

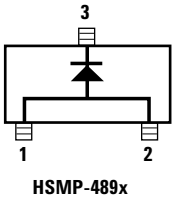


Figure 16. Internal Connections.

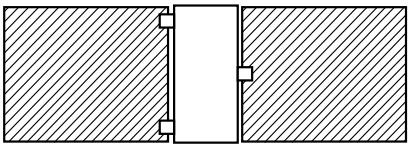


Figure 17. Circuit Layout.

Microstrip Shunt Connections for HSMP-489x Series

In Figure 18, the center conductor of the microstrip line is interrupted and leads 1 and 2 of the HSMP-489x diode are placed across the resulting gap. This forces the 1.5 nH lead inductance of leads 1 and 2 to appear as part of a low pass filter, reducing the shunt parasitic inductance and increasing the maximum available attenuation. The 0.3 nH of shunt inductance external to the diode is created by the via holes, and is a good estimate for 0.032" thick material.

Co-Planar Waveguide Shunt Connection for HSMP-489x Series

Co-Planar waveguide, with ground on the top side of the printed circuit board, is shown in Figure 20. Since it eliminates the need for via holes to ground, it offers lower shunt parasitic inductance and higher maximum attenuation when compared to a microstrip circuit.

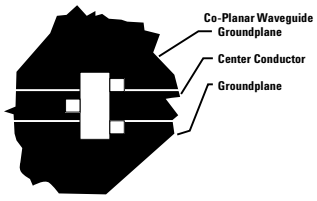


Figure 20. Circuit Layout.

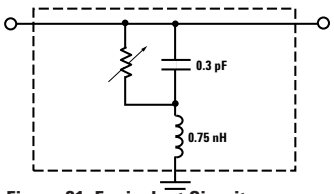


Figure 21. Equivalent Circuit.

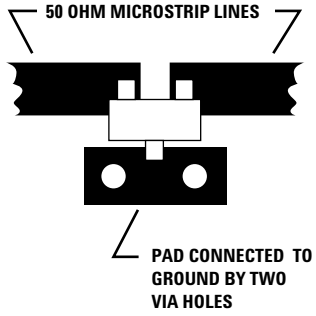


Figure 18. Circuit Layout.

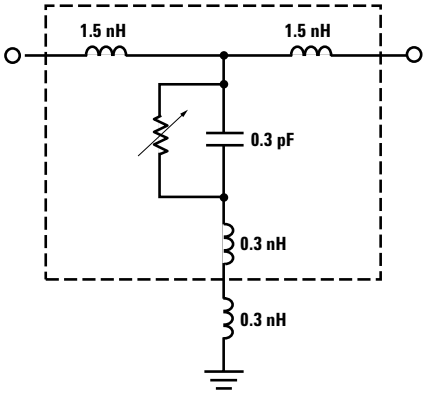
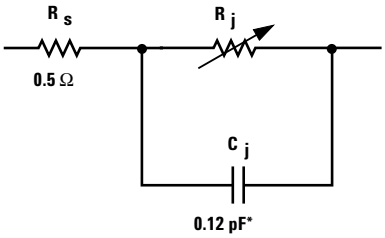


Figure 19. Equivalent Circuit.

Equivalent Circuit Model: HSMP-389x Chip*



*** Measured at -20 V**

$R_T = 0.5 + R_j$

$C_T = C_P + R_j$

$R_j = \frac{20}{I^{0.9}}\ \Omega$

I = Forward Bias Current in mA

*** See AN1124 for package models**

A SPICE model is not available for PIN diodes as SPICE does not provide for a key PIN diode characteristic, carrier lifetime.

Assembly Information

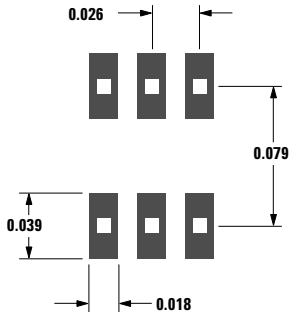


Figure 22. Recommended PCB Pad Layout for Avago Technologies' SC70 6L / SOT-363 Products.

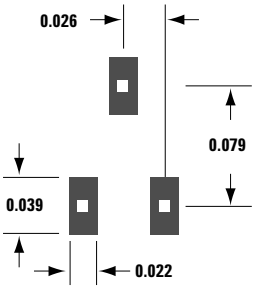


Figure 23. Recommended PCB Pad Layout for Avago Technologies' SC70 3L / SOT-323 Products.

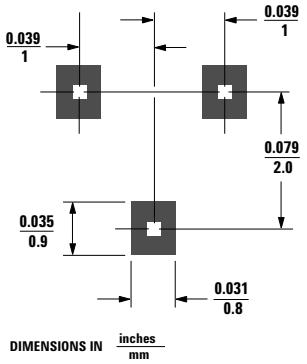


Figure 24. Recommended PCB Pad Layout for Avago Technologies' SOT-23 Products.

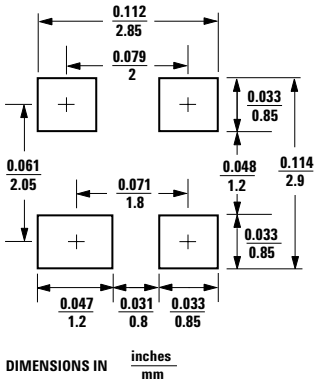


Figure 25. Recommended PCB Pad Layout for Avago Technologies' SOT-143 Products.

SMT Assembly

Reliable assembly of surface mount components is a complex process that involves many material, process, and equipment factors, including: method of heating (e.g., IR or vapor phase reflow, wave soldering, etc.) circuit board material, conductor thickness and pattern, type of solder alloy, and the thermal conductivity and thermal mass of components. Components with a low mass, such as the SOT package, will reach solder reflow temperatures faster than those with a greater mass.

Avago Technologies' diodes have been qualified to the time-temperature profile shown in Figure 26. This profile is representative of an IR reflow type of surface mount assembly process.

After ramping up from room temperature, the circuit board with components attached to it (held in place with solder paste) passes through one or more preheat zones. The preheat zones increase the temperature of the board and components to prevent thermal shock and begin evaporating solvents from the solder paste. The reflow zone briefly elevates the temperature sufficiently to produce a reflow of the solder.

The rates of change of temperature for the ramp-up and cool-down zones are chosen to be low enough to not cause deformation of the board or damage to components due to thermal shock. The maximum temperature in the reflow zone (T_{MAX}) should not exceed 235°C.

These parameters are typical for a surface mount assembly process for Avago Technologies diodes. As a general guideline, the circuit board and components should be exposed only to the minimum temperatures and times necessary to achieve a uniform reflow of solder.

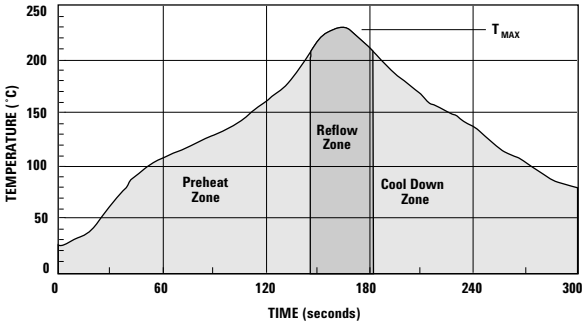
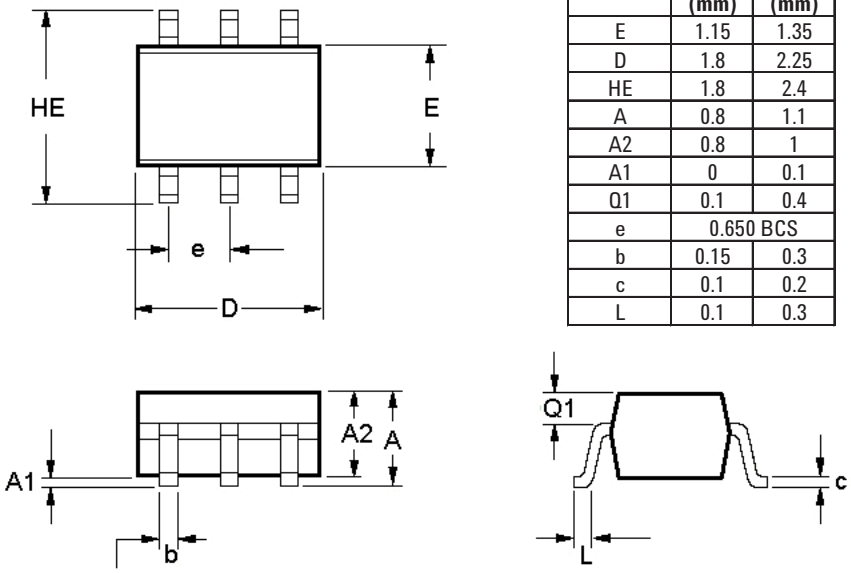


Figure 26. Surface Mount Assembly Profile.

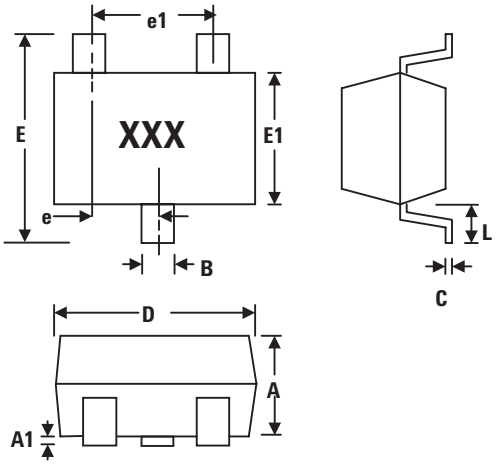
Package Dimensions

Outline SOT-363 (SC-70 6 Lead)



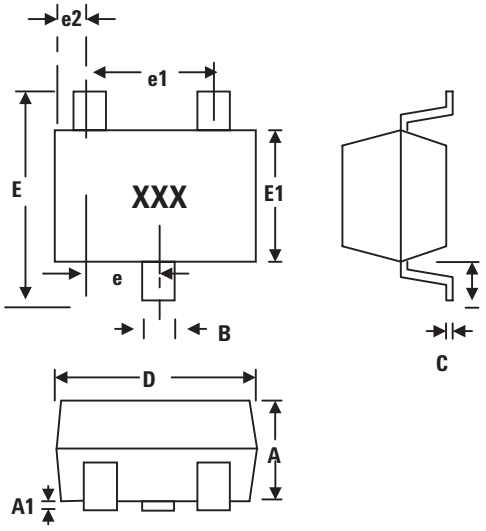
Symbol	Agilent (New)	
	MIN (mm)	MAX (mm)
E	1.15	1.35
D	1.8	2.25
HE	1.8	2.4
A	0.8	1.1
A2	0.8	1
A1	0	0.1
Q1	0.1	0.4
e	0.650 BCS	
b	0.15	0.3
c	0.1	0.2
L	0.1	0.3

Outline SOT-323 (SC-70 3 Lead)



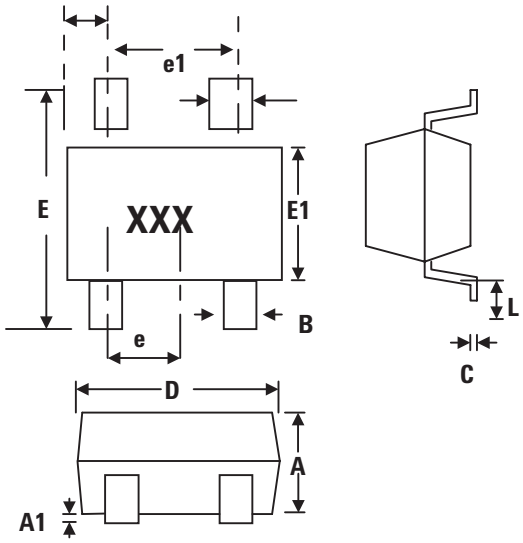
SYMBOL	AGILENT	
	MIN	MAX
A	0.8	1
A1	0	0.1
B	0.15	0.4
C	0.1	0.2
D	1.8	2.25
E1	1.1	1.4
e	0.65 typical	
e1	1.30 typical	
E	1.8	2.4
L	0.425 typical	

Outline 23 (SOT-23)



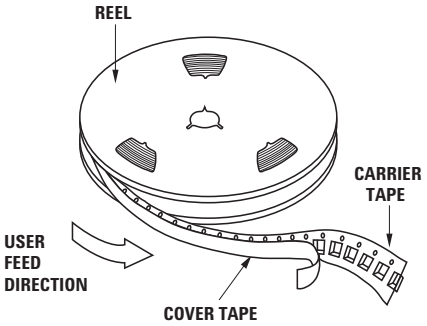
SYMBOL	AGILENT	
	MIN	MAX
A	0.79	1.2
A1	0	0.1
B	0.37	0.54
C	0.086	0.152
D	2.73	3.13
E1	1.15	1.5
e	0.89	1.02
e1	1.78	2.04
e2	0.45	0.6
E	2.1	2.7
L	0.45	0.69

Outline 143 (SOT-143)

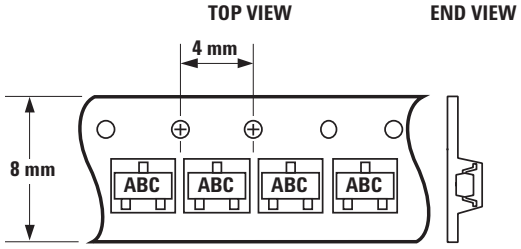


	AGILENT	
SYMBOL	MIN	MAX
A	0.79	1.097
A1	0.013	0.1
B	0.36	0.54
B1	0.76	0.92
C	0.086	0.152
D	2.8	3.06
E1	1.2	1.4
e	0.89	1.02
e1	1.78	2.04
e2	0.45	0.6
E	2.1	2.65
L	0.45	0.69

Device Orientation

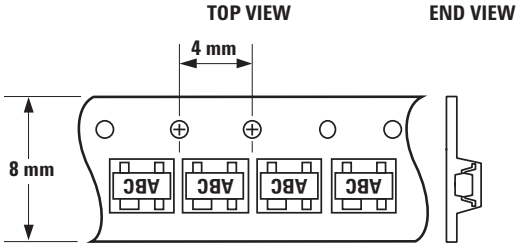


For Outlines SOT-23, -323



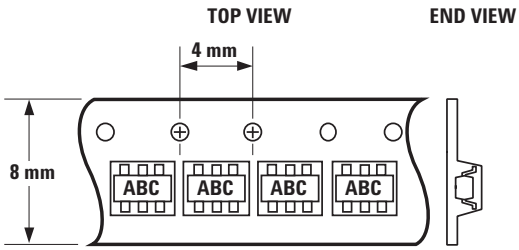
Note: "AB" represents package marking code.
"C" represents date code.

For Outline SOT-143



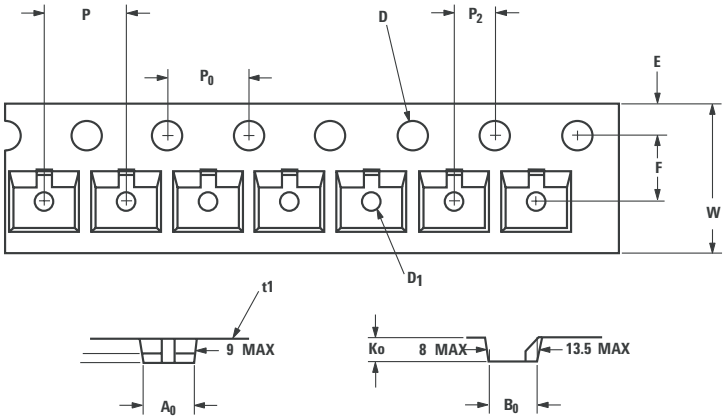
Note: "AB" represents package marking code.
"C" represents date code.

For Outline SOT-363



Note: "AB" represents package marking code.
"C" represents date code.

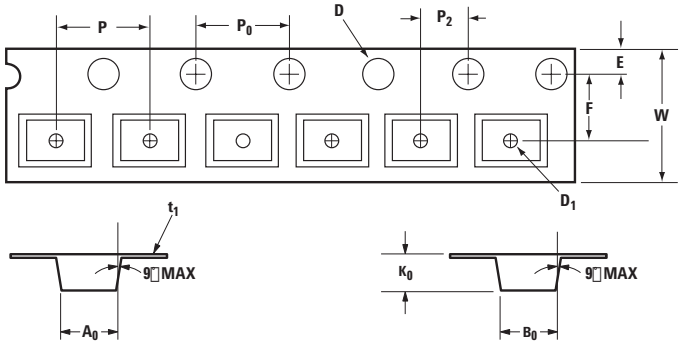
Tape Dimensions and Product Orientation
For Outline SOT-23



DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A_0	3.15 ± 0.10	0.124 ± 0.004
	WIDTH	B_0	2.77 ± 0.10	0.109 ± 0.004
	DEPTH	K_0	1.22 ± 0.10	0.048 ± 0.004
	PITCH	P	4.00 ± 0.10	0.157 ± 0.004
	BOTTOM HOLE DIAMETER	D_1	1.00+ 0.05	0.039 ± 0.002
PERFORATION	DIAMETER	D	1.50 + 0.10	0.059 + 0.004
	PITCH	P_0	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	8.00 +0.30 –0.10	0.315 +0.012 -0.004
	THICKNESS	t1	0.229 ±0.013	0.009 ±0.0005
DISTANCE BETWEEN CENTERLINE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	3.50 0.05	0.138 ±0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ±0.05	0.079 ±0.002

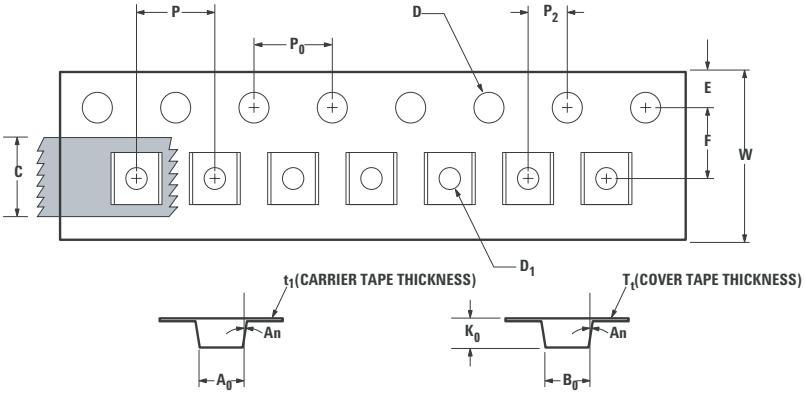
Tape Dimensions and Product Orientation

For Outline SOT-143



DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A_0	3.19 ± 0.10	0.126 ± 0.004
	WIDTH	B_0	2.80 ± 0.10	0.110 ± 0.004
	DEPTH	K_0	1.31 ± 0.10	0.052 ± 0.004
	PITCH	P	4.00 ± 0.10	0.157 ± 0.004
	BOTTOM HOLE DIAMETER	D_1	1.00 + 0.25	0.039 + 0.010
PERFORATION	DIAMETER	D	1.50 + 0.10	0.059 + 0.004
	PITCH	P_0	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	8.00 +0.30 –0.10	0.315+0.012 –0.004
	THICKNESS	t1	0.254 ± 0.013	0.0100 ± 0.0005
DISTANCE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	3.50 ± 0.05	0.138 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ± 0.05	0.079 ± 0.002

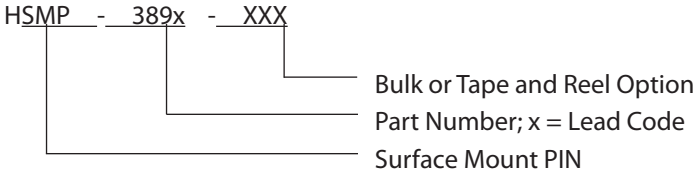
For Outlines SOT-323, -363



DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A_0	2.40 ± 0.10	0.094 ± 0.004
	WIDTH	B_0	2.40 ± 0.10	0.094 ± 0.004
	DEPTH	K_0	1.20 ± 0.10	0.047 ± 0.004
	PITCH	P	4.00 ± 0.10	0.157 ± 0.004
	BOTTOM HOLE DIAMETER	D_1	1.00 + 0.25	0.039 + 0.010
PERFORATION	DIAMETER	D	1.55 ± 0.05	0.061 ± 0.002
	PITCH	P_0	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	8.00 ± 0.30	0.315 ± 0.012
	THICKNESS	t_1	0.254 ± 0.02	0.0100 ± 0.0008
COVER TAPE	WIDTH	C	5.4 ± 0.10	0.205 ± 0.004
	TAPE THICKNESS	T_t	0.062 ± 0.001	0.0025 ± 0.00004
DISTANCE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	3.50 ± 0.05	0.138 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ± 0.05	0.079 ± 0.002
ANGLE	FOR SOT-323 (SC70-3 LEAD)	An	8° MAX	
	FOR SOT-363 (SC70-6 LEAD)		10° MAX	

Ordering Information

Specify part number followed by option. For example:



Option Descriptions

-BLK = Bulk, 100 pcs. per antistatic bag
-TR1 = Tape and Reel, 3000 devices per 7" reel
-TR2 = Tape and Reel, 10,000 devices per 13" reel

Tape and Reeling conforms to Electronic Industries RS-481, "Taping of Surface Mounted Components for Automated Placement."

For lead-free option, the part number will have the character "G" at the end, eg. -TR2G for a 10K pc lead-free reel.

Package Characteristics

Lead Material ..... Copper (SOT-323/363); Alloy 42 (SOT-23/143)
Lead Finish ..... Tin-Lead 85-15% (Non lead-free option)
..... Tin 100% (Lead-free option)
Maximum Soldering Temperature ..... 260°C for 5 seconds
Minimum Lead Strength..... 2 pounds pull
Typical Package Inductance ..... 2 nH
Typical Package Capacitance ..... 0.08 pF (opposite leads)

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

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5989-3860EN - March 29, 2006